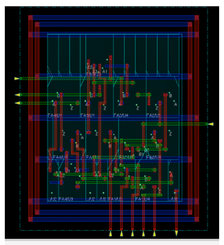
Low Power Nanoelectronics for Post-CMOS Reconfigurable ICs

Santosh Khasanvis, Csaba Andras Moritz, University of Massachusetts Amherst

Challenges with Existing Technology

- Technological: Arbitrary layouts & sizing; stringent overlay (3nm), variability (1.3nm CD) at 16nm node – ITRS 2011
- Power/Thermal
- Economic: Escalating manufacturing cost, design cost for custom IC development

CMOS Arbitrary Layouts



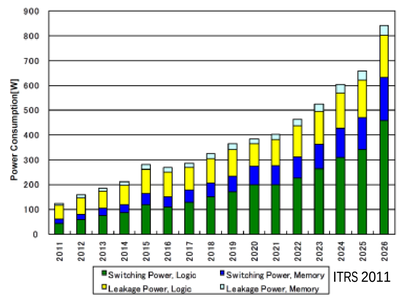
ITRS '11 CMOS Projections

Year	MPU Gate (nm)	Overlay 3σ (nm)	Gate CD 3σ (nm)
2013	28	5.4	2.1
2014	25	4.8	1.9
2015	22	4.2	1.7
2016	20	3.8	1.6
2017	18	3.4	1.5
2018	16	3	1.3
2019	14	2.7	1.2
2020	12	2.4	1.1
2021	11	2.1	1
2022	10	1.9	0.9
2023	8.8	1.7	0.8
2024	7.9	1.5	0.8

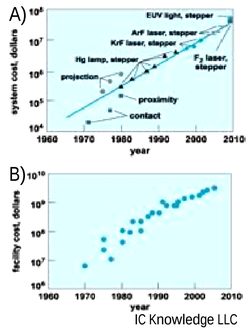
ITRS 2011

Legend: Manufacturing Solutions Known; Manufacturing Solutions Not Known

Power Consumption Trends



Trends in (A) Lithographic Tool Costs and (B) Facility Costs

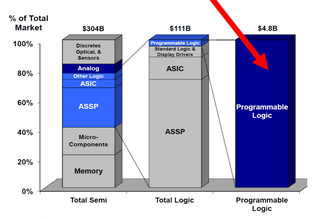


IC Knowledge LLC

Reconfigurable Computing

- Post-manufacturing programmability; Reduced time to market; Low design costs
- *Inefficient emulated reconfigurability*
- *Explore new paradigms: Emerging nanomaterials and phenomena*

Scope for Reconfigurable Systems



Source: Lattice Semi

Reconfigurable Nanowire Computing Fabric

New Material: Silicon Nanowires

FPGA: Emulated Reconfiguration

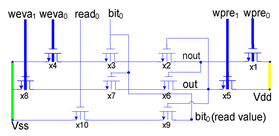
Reconfigurable Cross-Nanowire FET (xnwFET)

Chui Group, UCLA

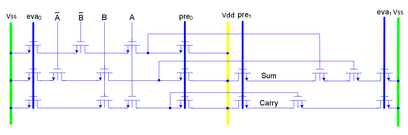
New Concepts

- Fine-grained reconfigurability at device-level
- Novel circuits for volatile memory/logic that can be mapped into uniform grid-based nanowire tiles

Volatile Memory Cell Circuit

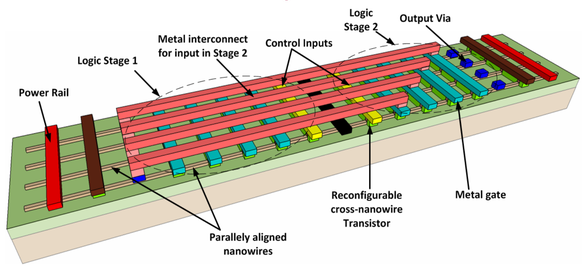


Logic Circuit (Adder)



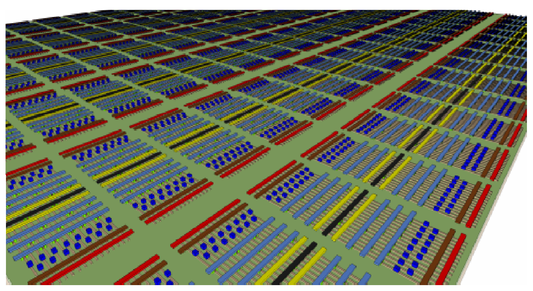
Can be mapped by programming certain crosspoints

Nanowire-based Reconfigurable Fabric: Nano-FPGA



Vision

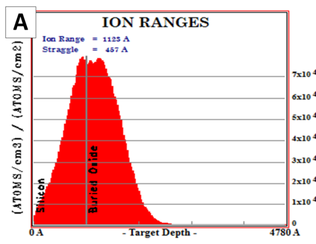
- Unified nanowire fabric for logic & memory targeting efficient, low-cost reconfigurable systems



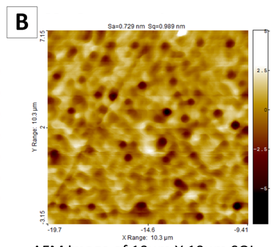
Benchmarking of WISP-0 Nanoprocessor

Nano-FPGA	Area	Power	Performance
Vs. Projected 16nm CMOS FPGAs	54x	50x	17x

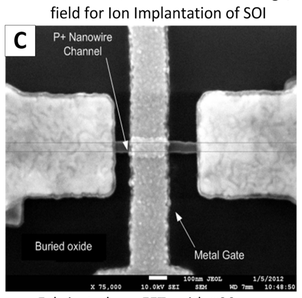
Experimental Effort



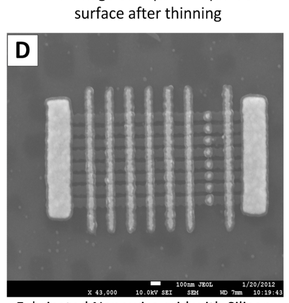
SRIM Simulations to determine dosage/ field for Ion Implantation of SOI



AFM image of 10μm X 10μm SOI surface after thinning



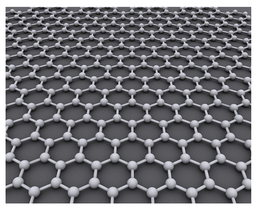
Fabricated xnwFETs with ~30nm nanowire width



Fabricated Nanowire grid with Silicon nanowires and orthogonal Ti gates

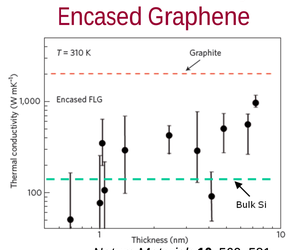
Thermal Management

Graphene



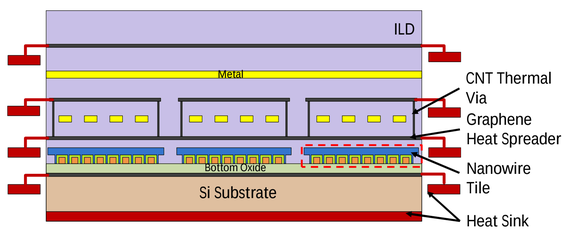
Source: Wikipedia

Thermal Conductivity of Encased Graphene



Nature Materials **10**, 569–581

Integrated Graphene Thermal Network

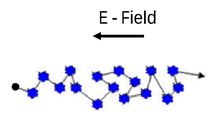


Balandin Group, UCR

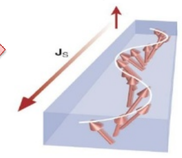
Spin Wave Functions

New Physical Phenomenon: Electron Spin

Current: Electrical Charge based Computation

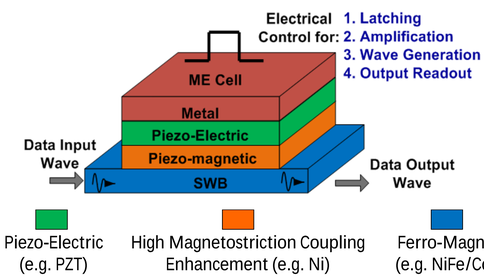


Proposed: Electron Spin based Computation



Nature **464**, 262-266

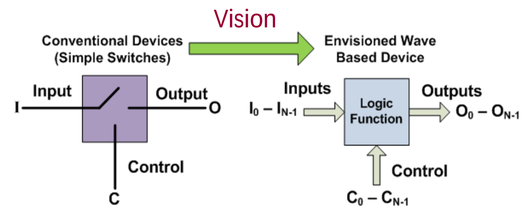
Magneto-Electric Cell



New Concepts

- Non-volatile computing: Logic & Memory
- Leveraging collective precession of spins in ferro-magnetic materials

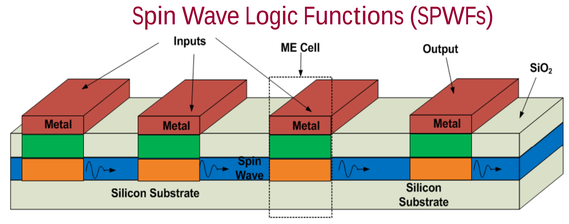
Vision



Vision: Spin Wave Functions (SPWFs)

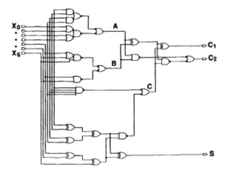
- Encode information in amplitude and phase of spin-wave; Computation based on wave superposition
- Multi-valued representation; No charge transport → Low power

Spin Wave Logic Functions (SPWFs)



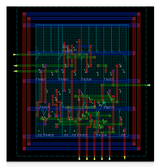
Benchmarking SPWF Logic vs. Other Approaches: 7/3 Counter

Conventional Boolean Logic (*Highly Complex*)

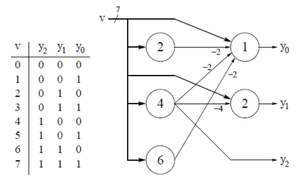


M. Mehta, et al., ARITH, pp. 43-50, 1991.

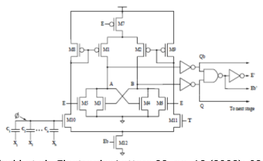
45nm Standard Cell Library based CMOS Layout for (7;3) Counter



Threshold Logic (*Few threshold gates, but individual gates Highly Complex*)

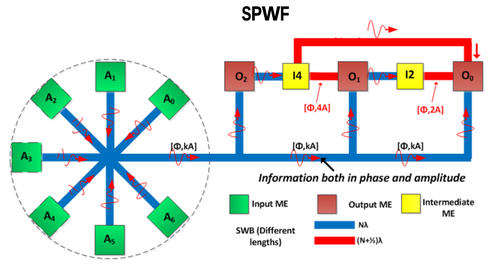


MOSFET based Threshold Logic Gate (*Highly Complex*)



P. Celinski et al., Electronics Letters 38, no. 13 (2002): 633-635.

SPWF



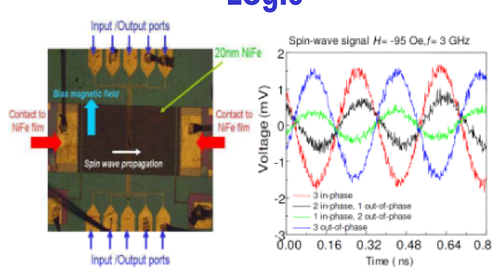
- *Significant reduction in logic complexity*

ME Cell Assumptions
- Switching delay: 100 ps
- Area: 100nm X 100nm
- Energy: 10 aJ/operation

Spin-Wave Bus Assumptions
- Velocity: 10^4 m/s
- Width/spacing: 100 nm/45 nm
- Min. Length: at least equal to wavelength of spin waves (λ)
- λ = 100nm

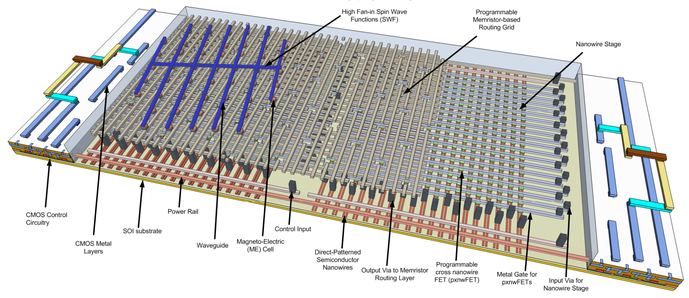
CMOS		
Area (μm²)	Delay (ps)	Power (μW)
27	740	14
SPWF		
Area (μm²)	Delay (ps)	Power (μW)
0.2	670	0.2

Experimental: Spin Wave Majority Logic



Khitun, UCR

Hybrid Spin-Charge Reconfigurable Fabric



FCRP · FENA · NSF National Science Foundation WHERE DISCOVERIES BEGIN · DARPA · CHM Center for Hierarchical Manufacturing